

## SANYO Semiconductors DATA SHEET

**LA5754** -

**Monolithic Linear IC** 

# Separately-excited Step-down Switching Regulator (Variable Type)

#### Overview

The LA5754 is a separately-excited step-down switching regulator (variable type).

#### **Features**

- High efficiency
- Four external parts
- Time-base generator (125kHz) incorporated
- Current limiter incorporated
- Thermal shutdown circuit incorporated
- Soft start circuit incorporated

#### **Specifications**

**Absolute Maximum Ratings** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V <sub>IN max</sub>		30	V
Output current	I <sub>O</sub> max		3	А
SW pin application reverse voltage	Vsw		-1	V
Allowable power dissipation	Pd max1	Infinite heat sink.	7.5	W
	Pd max2	No heat sink.	1.75	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-30 to +125	°C
Storage temperature	Tstg		-40 to +150	°C

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## **Recommended Operating Conditions** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage range	V <sub>IN</sub>		5.5 to 28	V
Operating junction temperature range	Тј ор		-30 to +150	°C

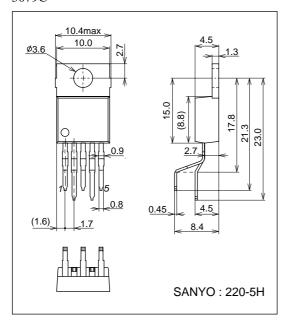
### **Electrical Characteristics** at Ta = 25°C

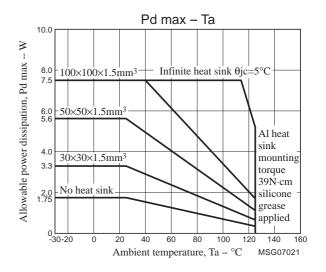
Parameter	Symbol	Conditions	Ratings			1.114
			min	typ	max	Unit
Output voltage	VO	V <sub>IN</sub> = 15V, I <sub>O</sub> = 1.0A	2.53	2.66	2.76	V
Switching frequency	f	V <sub>IN</sub> = 15V, I <sub>O</sub> = 1.0A	100	125	150	kHz
Line regulation	ΔVOLINE	V <sub>IN</sub> = 8 to 20V, I <sub>O</sub> =1.0A		25	80	mV
Load regulation	ΔVOLOAD	V <sub>IN</sub> = 15V, I <sub>O</sub> = 0.5 to 1.5A		10	30	mV
Output voltage temperature coefficient	ΔVΟ/ΔΤα			±0.5		mV/°C
Ripple attenuation factor	RREJ	f = 100 to 120Hz		45		dB
Current limiter operating voltage	IS	V <sub>IN</sub> = 15V	3.1			Α
Thermal shutdown operating temperature	TSD	Designed target value*		165		°C
Thermal shutdown hysteresis width	ΔTSD	Designed target value*		15		°C

<sup>\*</sup> Designed target value: No measurement made.

## **Package Dimensions**

unit : mm (typ) 3079C

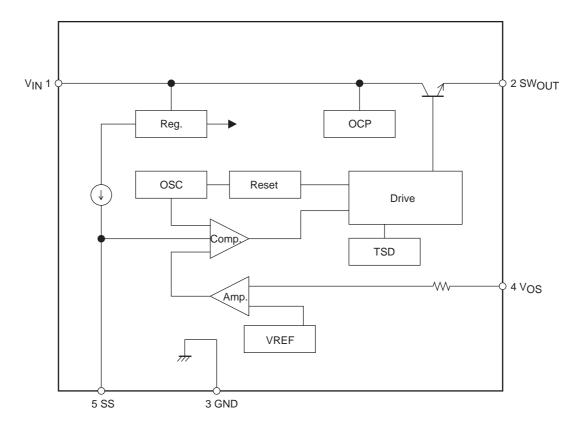




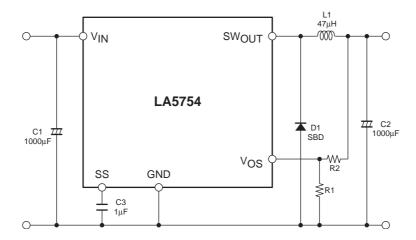
## **Pin Assignment**

 $(1)V_{\mbox{\footnotesize{IN}}}$   $(2)SW_{\mbox{\footnotesize{OUT}}}$  (3)GND  $(4)V_{\mbox{\footnotesize{OS}}}$  (5)SS

## **Block Diagram**



## **Application Circuit Example**



Notes: C3 is for the soft start function. Delete C3 and keep the SS pin open when the soft function is not necessary.

#### Calculation equation to set the output voltage

This IC controls the switching output so that the  $V_{\mbox{OS}}$  pin voltage becomes 2.66V (typ).

The equation to set the output voltage is as follows:

$$V_O = \left(1 + \frac{R2}{RI}\right) \times 2.66V(typ)$$

The  $V_{\mbox{OS}}$  pin has the inrush current of  $1\mu\mbox{A}$  (typ). Therefore, the error becomes larger when R1 and R2 resistance values are large.

## **Description of Functional Settings**

#### 1.Start delay function

The SS pin has the internally-connected  $22\mu A$  (typ) constant-current supply. When the voltage of SS pin exceeds the threshold voltage, the regulator starts operation. As the threshold is 0.62V(typ), the start delay time can be calculated as follows:

ex. For setting at 1µF

$$Td = \frac{C \times V}{i} = \frac{I\mu \times 0.62}{22\mu} = 28.2 \; msec$$

#### 2.Soft start function

The internal PWM waveform has the voltage value as shown in the right. If down-conversion from the voltage of  $V_{IN} = 15V$  to 3.3V output to be made, for example, the PWM-ON duty has the value as shown below.



$$PWMduty = \frac{VOUT + VF}{VIN - Vsat + VF} = 25\%$$

(Note that calculation is made with Vsat = 1V and VF = 0.2V)

The output voltage of error amplifier, which is 3.3V, is the value with PWM = 25%, as calculated in the above equation, so that this voltage is determined as follows:

 $Ver = (\Delta VPWM) \times PWMduty + VPWML = 0.88V \times 0.25 + 0.62V = 0.84V$ ( $\Delta VPWM$  is the PWM amplitude value or 0.88V(typ) while VPWML is the lower limit voltage of PWM waveform or 0.62V(typ))

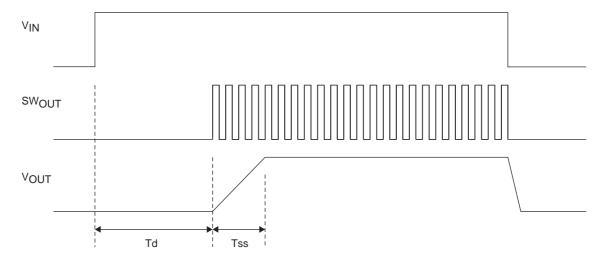
SS pin and error amplifier output voltages are designed to prefer the lower voltages, so that V<sub>OUT</sub> will reach the designed regulation voltage in timing when the SS pin voltage exceeds the error amplifier output. Therefore, the soft strt time is calculated as follows:

$$Tss = \frac{C \times \Delta VPWM \times PWMduty}{i} = \frac{C \times 0.88 \times PWMduty}{22uA}$$

For the set conditions of  $C = 1\mu F$  and PWMduty = 25%:

$$\mathit{Tss} = \frac{1\mu \times 0.88V \times 0.25}{22\mu A} = 10 \mathit{msec}$$

## **Timing Chart**



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